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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,728	02/06/2004	Jingang Wu	021653-004200US	8605

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EXAMINER	
LUK, OLIVIA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,728	WU ET AL.	
	Examiner	Art Unit	
	Olivia T. Luk	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al. (4,181,538) in view of Wack et al. (6,818,459 B2).

In re claim 1, Narayan et al. discloses providing a monitor wafer (col. 4, line 37), the monitor wafer comprising a silicon material (col. 4, line 37); introducing a plurality of particles within a depth of the silicon material (col. 12, lines 22-25), whereupon the plurality of particles cause the silicon material to be in an amorphous state (col. 12, lines 22-25); introducing a plurality of dopant particles into a selected depth of the silicon material using an implantation tool (col. 4, lines 43-50), the amorphous state trapping the dopant particles (col. 4, lines 43-50); subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant (col. 4, lines 59-61); removing the monitor wafer, measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer (col. 4, lines 62-66); determining a dose of the dopant bearing impurities (col. 6, lines 36-50); but fails to teach operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

Wack et al. teaches a measurement and detection system for semiconductor processing that includes detecting defects, deposition material thickness, a sheet resistivity of a deposited material, a thermal diffusivity of a deposited material, or any combination thereof for the purpose of controlling the deposition process (bridging paragraph between col. 111 and col. 112).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the determination of a dose of the dopant bearing impurities and sheet resistivity from Table I of Narayan et al. to control the operation of an implantation tool using one of more production wafers if the does of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

In re claim 2, Narayan et al. further discloses the monitor wafer is substantially free of screen oxide overlying a surface of the monitor wafer (col. 3, lines 55-60).

In re claim 3, Narayan et al. further discloses the plurality of particles are silicon bearing impurities (col. 9, lines 15-30).

In re claim 4, Narayan et al. in view of Wack et al. is applied as above, but fails to teach the silicon bearing impurities are implanted using a dose of 1×10^{15} atoms/cm^2 and an energy of 20 keV.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have implanted the silicon bearing impurities using a dose of 1×10^{15} atoms/cm^2 and an energy of 20 keV, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In re claim 5, Narayan et al. further discloses the dopant particles are boron bearing impurities (col. 4, lines 44-47).

In re claim 6, Narayan et al. in view of Wack et al. is applied as above, but fails to teach the boron bearing impurities are implanted using a dose ranging from about 5×10^{13} through 4×10^{14} atoms/cm^2 and an energy ranging from about 1-2 keV.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have implanted the boron bearing impurities are implanted using a dose ranging from about 5×10^{13} through 4×10^{14} atoms/cm^2 and an energy ranging from about 1-2 keV, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In re claims 7-9, Narayan et al. further discloses the thermal anneal process but fails to teach it is a rapid thermal anneal process at about 700 or ranging from about 650 to 750 Degrees Celsius.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the thermal anneal process is an RTP process at about 700 or ranging from about 650 to 750 Degrees Celsius, since the RTP process is well known in the art and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In re claim 10, Narayan et al. in view of Wack et al. is applied as above, Wack et al. further teaches sheet resistivity is provided in a separate tool (col. 112, lines 1-7).

In re claim 11, Narayan et al. in view of Wack et al. is applied as above, but fails to specify operating of the production wafers occurs for 24 hours after determining the dose of the dopant impurities.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have operated the production wafers for 24 hours after determining the dose of the dopant impurities for efficient production of semiconductors.

In re claim 12, Narayan et al. discloses the thermal anneal process also recrystallizes a portion of the amorphous silicon (col. 6, lines 40-50).

In re claim 13, Narayan et al. discloses providing a monitor wafer (col. 4, line 37), the monitor wafer comprising a crystalline material (col. 4, line 37); introducing a plurality of particles within a depth of the material (col. 12, lines 22-25), whereupon the plurality of panicles cause the crystalline material to be in an amorphous state (col. 12, lines 22-25); introducing a plurality of dopant particles into a selected depth of the crystalline material using an implantation tool (col. 4, lines 43-50), the amorphous state trapping the dopant particles (col. 4, lines 43-50); subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant (col. 4, lines 59-61); removing the monitor wafer, measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer (col. 4, lines 62-66); determining a dose of the dopant bearing impurities (col. 6, lines 36-50); but fails to teach operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

Wack et al. teaches a measurement and detection system for semiconductor processing that includes detecting defects, deposition material thickness, a sheet resistivity of a deposited material, a thermal diffusivity of a deposited material, or any combination thereof for the purpose of controlling the deposition process (bridging paragraph between col. 111 and col. 112).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the determination of a dose of the dopant bearing impurities and sheet resistivity from Table I of Narayan et al. to control the operation of an implantation tool using one of more production wafers if the does of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

In re claim 13, Narayan et al. further discloses the crystalline material comprises silicon (col. 4, line 36).

In re claim 14, Narayan et al. further discloses the dose of the dopant bearing impurities is determined using a relationship between resistivity values and dose values (Table I).

In re claim 15, Narayan et al. does not provide a spatial plot of the relationship, but this plot can inherently be made from Table I.

In re claim 16, Narayan et al. discloses the plurality of particles comprise silicon bearing particles (col. 9, lines 15-30).

In re claim 17, Narayan et al. discloses the dopant bearing impurities comprises boron species (col. 4, lines 44-50).

In re claim 18, Narayan et al. further discloses the monitor wafer is substantially free from an overlying oxide layer before introducing the dopant bearing impurities (col. 3, lines 55-60).

In re claim 19, Narayan et al. further discloses the monitor wafer is silicon wafer (col. 4, line 37).

In re claim 20, Narayan does not specify that one of more production wafers is characterized by a shallow junction depth of less than about 40 nm, but it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a shallow junction depth of less than about 40 nm for any number of the production wafers as it is well known in the art that measurement of sheet resistivity and controlling of deposition tools may be utilized on wafers with a shallow junction depth of less than about 40 nm.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References not applied are considered state of the art in the area of semiconductor manufacture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Olivia T. Luk whose telephone number is 571-272-1676. The examiner can normally be reached on 8AM to 5PM Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

OTL
February 15, 2005

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER